

This listing of claims will replace all prior versions,
and listings, of claims in the application:

Claims 1-17 (canceled)

1 Claim 18 (currently amended): A solid-state image
2 sensing apparatus comprising:
3 an image sensing area in which a plurality of pixels
4 are two-dimensionally arrayed;
5 a plurality of output channels;
6 a first driving mode in which pixel signals of
7 pixels in the image sensing area are read out, wherein
8 the read-out pixel signals are output to at least one
9 output channel selected from among the plurality of
10 output channels;
11 a second driving mode in which pixel signals of
12 odd-numbered columns and pixel signals of even-numbered
13 columns arrayed in the same row in the image sensing area
14 are read-out, wherein the read-out pixel signals are
15 output to a plurality of output channels selected from
16 among the output channels, and wherein the read-out pixel
17 signals of odd-numbered columns and the read-out pixel
18 signals of even-numbered columns are output to different
19 ones of the selected output channels so as to have
20 different phases; ~~[[and]]~~
21 line memories which are arranged between the pixels
22 and the output channels and which temporarily store pixel
23 signals of the pixels selected and read out in the first
24 driving mode or the second driving mode; and
25 a control circuit which is arranged between the
26 pixels and the line memories and which sets a driving
27 mode to one of the first driving mode and the second

28 driving mode based on an externally input signal ~~for~~
29 ~~wherein the input signal]]~~ which may be freely set,
30 wherein the number of output channels to which the
31 pixel signals are output in the first driving mode and
32 the number of output channels to which the pixel signals
33 are output in the second driving mode are different.

1 Claim 19 (currently amended): The solid-state image
2 sensing apparatus according to claim 18, ~~[[further~~
3 ~~comprising line memories which temporarily store selected~~
4 ~~and read out pixel signals of pixels,]]~~
5 wherein the control circuit ~~[[is arranged between~~
6 ~~the pixels and the line memories and]]~~ is a transfer
7 switch in which a common control signal is input in every
8 other column.

1 Claim 20 (previously presented): The solid-state image
2 sensing apparatus according to claim 18, wherein the
3 phase shift between the pixel signals of the odd-numbered
4 columns and the pixel signals of the even-numbered
5 columns is 180 degrees.

1 Claim 21 (previously presented): The solid-state image
2 sensing apparatus according to claim 18,
3 wherein the image sensing area is provided with a
4 color filter in Bayer matrix corresponding to the pixels,
5 and
6 in the second driving mode, pixel signals of pixels
7 in the same color phase among color phase codings defined
8 by the color filters are output from the same output
9 channels.

1 Claim 22 (previously presented): The solid-state image
2 sensing apparatus according to claim 18, wherein in the
3 first and second driving modes, there is a channel which
4 can be used in common.

1 Claim 23 (previously presented): The solid-state image
2 sensing apparatus according to claim 18, wherein in both
3 the first and second driving modes, pixel signals of
4 pixels from $m \times n$ pieces in the image sensing area are
5 output wherein m and n are integers.

1 Claim 24 (new): The solid-state image sensing apparatus
2 according to claim 18, wherein the line memories are
3 capacitive elements arranged in every column.